

WHAT IS CLAIMED:

1 1. A method including:

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3 dedicating a first portion of a resource exclusively to a first thread;

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5 dedicating a second portion of the resource exclusively to a second

6 thread; and

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8 dynamically sharing a third portion of the resource between the first

9 and second threads.

1 2. The method of claim 1 wherein the dynamic sharing of the third

2 portion of the resource is performed according to resource demands of the

3 respective first and second threads.

1 3. The method of claim 1 wherein the resource comprises a memory

2 resource including first and second portions dedicated to the first and

3 second threads respectively and a third portion shared between the first and

4 second threads, the method including:

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6 identifying a first location within the memory resource as a candidate

7 location to receive an information item associated with the first

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8 thread;

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10 determining whether the candidate location is within the first or the
11 third portion of the memory resource dedicated to the first thread;

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12 if the candidate location is within the first or the third portion of the
13 memory resource, then storing the information associated the first
14 thread at the candidate location; and

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16

17 if the candidate location is within the second portion of the memory
18 resource then identifying a further location as being the candidate
19 location.

1 4. The method of claim 3 wherein the memory resource comprise a N
2 way set associative memory and wherein the first portion comprises a first
3 way dedicated to the first thread, the second portion comprises a second
4 way dedicated to the second thread and the third portion comprises a third
5 way shared between the first and second threads, wherein the identification
6 of the first location as the candidate location comprises identifying a selected
7 way within a selected set of the memory as a candidate way to receive the
8 information item associated with the first thread.

1 5. The method of claim 4 wherein the identification of the further

2 location as the candidate location comprises identifying a further way within
3 the selected set of the memory as the candidate way to receive the
4 information item associated with the first thread.

1 6. The method of claim 4 wherein the identification of the selected way
2 within the selected set as the candidate way comprises identifying a way
3 within the select set that was least recently used.

1 7. The method if claim 5 wherein the identification of the further way
2 within the selected set a candidate way comprises identifying a way within
3 the selected set that was second-least recently used.

1 8. The method of claim 6 including examining a Least Recently Used
2 (LRU) history for the selected set to identify the way that was least recently
3 used.

1 9. The method of claim 8 including examining a set of entries within the
2 LRU history for the selected set, each entry within the set of entries
3 indicating a respective way within the selected set, wherein the set of entries
4 is ordered in a sequence determined by least recent usage of a respective
5 way and the selection of the candidate way comprises performing a
6 sequential examination of the entries of the set of entries to locate a least
7 recently used way that comprises either the first or the second way.

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1 10. The method of claim 4 wherein memory comprises a trace cache
2 memory, and wherein the information item associated with the first thread
3 comprises a microinstruction of the first thread.

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1 11. A resource comprising:

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3 a first portion dedicated for utilization by a first thread executing
4 within a multi-threaded processor;

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6 a second portion dedicated to utilization by a second thread
7 executing within the multi-threaded processor; and

8
9 a third portion shared by the first and second threads.

1 12. The resource of claim 11 wherein the resource comprises a memory
2 including selection logic to identify a first location selection logic to identify
3 a first location within the memory resource as a candidate location to receive
4 an information item associated with the first thread, to determine whether
5 the candidate location is within the first or third portions of the memory
6 resource, then to store the information associated the first thread at the
7 candidate location but, if candidate location is within the second portion of
8 the memory resource, then to identify a further location as being the

9 candidate location.

1 13. The resource of claim 12 comprising a N way set associative memory
2 and within the first portion comprises a first way dedicated to the first
3 thread, the second portion comprises a second way dedicated to the second
4 thread and the third portion comprises a third way shared between the first
5 and second threads.

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1 14. The resource of claim 12 wherein the selection logic identifies a
2 selected way within a selected set of the memory as a candidate way to
3 receive the information item associated with the first thread if the selected
4 way comprises either the first or the third say.

1 15. The resource of claim 12 wherein the selection logic identifies a
2 further way within the selected set of the memory as the candidate way to
3 receive the information item associated with the first thread if the selected
4 way comprises the second way.

1 16. The resource of claim 14 wherein the selection logic identifies the
2 selected way within the selected set as the candidate way by identifying the
3 selected way within the select set as a last recently used way within the
4 selected set.

1 17. The resource of claim 15 wherein the selection logic identifies the
2 further way within the selected set a candidate way by identifying the
3 further way within the selected set as a second-least recently used way
4 within the selected set.

1 18. The resource of claim 16 wherein the selection logic examines a Least
2 Recently Used (LRU) history for the selected set to identify the way that was
3 least recently used.

1 19. The resource of claim 18 wherein the selection logic examines a set of
2 entries within the LRU history for the selected set, each entry within the set
3 of entries indicating a respective way within the selected set, wherein the set
4 of entries is ordered in a sequence determined by least recent usage of a
5 respective way and the selection of the candidate way comprises performing
6 a sequential examination of the entries of the set of entries to locate a least
7 recently used way that comprises either the first or the second way.

1 20. The resource of claim 18 wherein the memory comprising a trace
2 cache memory, and wherein the information item associated with the first
3 thread comprises a microinstruction of the first thread.

1 21. Selection logic including:
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3 first means for identifying a first location within a memory resource,
4 associated with a multi-threaded processor as a candidate location to
5 receive an information item associated with a first thread;

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7 second means for determining whether the candidate location is
8 within a second portion of the memory resource dedicated to the
9 second thread;

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11 wherein, if the candidate location is within the second portion of the
12 memory resource dedicated to second thread, the first means identifies a
13 further location within the memory resource as the candidate location.

1 22. The selection logic of claim 21 wherein the memory resource
2 comprises an N way set associative memory and wherein the first portion
3 comprises a first way dedicated to the first thread, the second portion
4 comprises a second way dedicated to the second thread and the third
5 portion comprises a third way shared between the first and second threads,
6 and wherein the first means identifies a selected way within a selected set of
7 the memory as a candidate way to receive information not associated with
8 the first way.

1 23. The selection logic of claim 22 wherein the first means identifies a
2 further way within the selected set of the memory as the candidate way to

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1 2 3 4 5 6 7 8 9 10 11 12 13

3 receive information associated with the first thread.

1 24. A method including:

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3 defining a memory resource, associated with a multi-threaded
4 processor, to include first and second portions dedicated to the first
5 and second threads respectively and a third portion shared between
6 the first and second threads;

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8 for an information item associated with the first thread, examining a
9 history of least recently used portions to identify either the first or the
10 third portion as being a least recently used portion available to the
11 first thread; and

12

13 storing the information item within the least recently used portion.

1 25. The method of claim 24 wherein, for the information item associated
2 with the first thread, the second portion is excluded from the identification
3 as the least recently used portion on account of being dedicated to the second
4 thread.

1 26. The method of claim 24, wherein the memory resource comprises a N
2 way set associative cache memory and wherein the first, second and third

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3 portions comprising respective first, second and third ways.

1 27. The method of claim 26 wherein the examination of the history of
2 least recently used portions includes examining a least recently used history
3 for a selected set of the set associative cache memory.

1 28. The method of claim 24 wherein the cache memory comprises a trace
2 cache memory, and wherein the information item associated with the first
3 thread comprises a microinstruction of the first thread.

1 29. A computer-readable medium storing a sequence of instructions that,
2 when executed within a processor, causes the processor to perform the steps
3 of:

4
5 dedicating a first portion of a resource exclusively to a first thread;

6
7 dedicating a second portion of the resource exclusively to a second
8 thread; and

9
10 dynamically sharing a third portion of the resource between the first
11 and second threads.

1 30. The computer readable medium of claim 29 wherein the dynamic

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- 2 sharing of the third portion of the resources is performed according to
- 3 resource demands of the respective first and second threads.